CLAIMS

1. An integrated circuit comprising:

a first node;

a second node;

a resistor coupling together the first and second nodes;

a comparator having two inputs and an output, a first one of the two inputs coupled to the resistor and the first node; and

a three-terminal device having a first terminal coupled to the second node and the resistor and having a second terminal coupled to the output of the comparator.

2. The integrated circuit of claim 1 wherein:

a second one of the two inputs of the comparator coupled to a first substantially constant voltage; and

a third terminal of the three-terminal device coupled to a second substantially constant voltage.

3. The integrated circuit of claim 2 wherein:

the first substantially constant voltage is provided by a voltage supply; and

the second substantially constant voltage is a ground potential.

4. The integrated circuit of claim 2 wherein:

the three-terminal device is a MOSFET;

the first terminal of the three-terminal device is a drain electrode of the MOSFET;

the second terminal of the three-terminal device is a gate electrode of the MOSFET; and

the third terminal of the three-terminal device is a source electrode of the MOSFET.

5. The integrated circuit of claim 1 wherein:

the three-terminal device is a MOSFET;

the first terminal of the three-terminal device is a drain electrode of the MOSFET; and

the second terminal of the three-terminal device is a gate electrode of the MOSFET.

6. The integrated circuit of claim 1 wherein:

a magnitude of a voltage at the second node is less than a magnitude of a voltage at a second one of the two inputs of the comparator.

7. The integrated circuit of claim 1 wherein:

the second terminal of the three-terminal device is a control electrode; and

the three-terminal device is turned on by the control electrode when a magnitude of a voltage at the first node is greater than a magnitude of a voltage at a second one of the two inputs of the comparator.

8. The integrated circuit of claim 1 wherein:

when a magnitude of a voltage at the first node is greater than a magnitude of a voltage at a second one of the two inputs of the comparator, the three-terminal device turns on to reduce a magnitude of a voltage at the second node to be less than or equal to the magnitude of the voltage at the second one of the two inputs of the comparator.

9. The integrated circuit of claim 1 further comprising:

an input signal coupled to the first node.

10. The integrated circuit of claim 9 further comprising:

a voltage-sensitive circuit coupled to the second node,

wherein:

the voltage-sensitive circuit processes the input signal.

11. An integrated circuit comprising:

a first circuit;

a first node; and

a second circuit coupling the first circuit to the first node;

wherein:

the first circuit operates off of a supply voltage; and

the second circuit detects a voltage magnitude of a signal at the first node and reduces the voltage magnitude of the signal to equal a voltage magnitude of the supply voltage before transmitting the signal to the first circuit.

12. The integrated circuit of claim 11 further comprising:

a second node; and

a third circuit coupling the first circuit to the second node;

wherein:

the third circuit detects a voltage magnitude of a different signal at the second node and reduces the voltage magnitude of the different signal to equal a voltage magnitude of the supply voltage before transmitting the different signal to the first circuit.

13. An integrated circuit comprising:

a first node;

a second node;

a first resistor coupling together the first and second nodes;

a first three-terminal device being of a first type, a first terminal of the first three-terminal device coupled to the first resistor and the first node;

a second three-terminal device being of the first type, a first terminal of the second three-terminal device coupled to a first substantially constant voltage, a second terminal of the second three-terminal device coupled to a second terminal of the first three-terminal device and to a third terminal of the second three-terminal device;

a third three-terminal device being of a second type, a first terminal of the third three-terminal device coupled to a second substantially constant voltage, a third terminal of the third three-terminal device coupled to a third terminal of the first three-terminal device;

a fourth three-terminal device being of the second type, a first terminal of the fourth three-terminal device coupled to the second substantially constant voltage, a second terminal of the fourth three-terminal device coupled to a second terminal of the third three-terminal device and to a third terminal of the fourth three-terminal device;

a fifth three-terminal device being of the second type, a first terminal of the fifth three-terminal device coupled to the second substantially constant voltage, a second terminal of the fifth three-terminal device coupled to the third terminals of the first and third three-terminal devices, a third terminal of the fifth three-terminal device coupled to the first resistor and to the second node;

a sixth three-terminal device being of the first type, a first terminal of the sixth three-terminal device coupled to the third terminals of the first and third three-terminal devices and to the second terminal of the fifth three-terminal device, a second terminal of the sixth three-terminal device coupled to the first substantially constant voltage, a third terminal of the sixth three-terminal device coupled to the second terminals of the third and fourth three-terminal devices and to the third terminal of the fourth three-terminal device; and

a second resistor coupling together the second terminals of the first and second three-terminal devices and the third terminal of the second three-terminal device to the second terminals of the third and fourth three-terminal devices and to the third terminals of the fourth and sixth three-terminal devices.

14. The integrated circuit of claim 13 wherein:

the first, second, third, fourth, fifth, and sixth three-terminal devices are MOSFETs.

15. The integrated circuit of claim 13 wherein:

the first, second, and sixth three-terminal devices are p-channel MOSFETs; and

the third, fourth, and fifth three-terminal devices are n-channel MOSFETs.

16. The integrated circuit of claim 15 wherein:

the first terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices are source electrodes;

the second terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices are gate electrodes; and

the third terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices are drain electrodes.

17. The integrated circuit of claim 13 further comprising:

a seventh three-terminal device, second and third terminals of the seventh three-terminal device coupled to the second terminal of the fifth three-terminal device, to the third terminals of the first and third three-terminal devices, and to the first terminal of the sixth three-terminal device.

18. The integrated circuit of claim 17 further comprising:

an eighth three-terminal device, a first terminal of the eighth three-terminal device coupled to the second substantially constant voltage, second and third terminals of the eighth three-terminal device coupled to a first terminal of the seventh three-terminal device.

19. The integrated circuit of claim 13 further comprising:

a third resistor coupling the first node and the first resistor to the first terminal of the first three-terminal device.

20. The integrated circuit of claim 19 further comprising:

a seventh three-terminal device, second and third terminals of the seventh three-terminal device coupled to the second terminal of the fifth three-terminal device, to the third terminals of the first and third three-terminal devices, and to the first terminal of the sixth three-terminal device; and

an eighth three-terminal device, a first terminal of the eighth three-terminal device coupled to the second substantially constant voltage, second and third terminals of the eighth three-terminal device coupled to a first terminal of the seventh three-terminal device.

21. The integrated circuit of claim 20 wherein:

the first, second, and sixth three-terminal devices are p-channel MOSFETs;

the third, fourth, and fifth three-terminal devices are n-channel MOSFETs;

the first terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices are source electrodes;

the second terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices are gate electrodes; and

the third terminals of the first, second, third, fourth, fifth, and sixth three-terminal devices are drain electrodes.

22. A method of operating an integrated circuit comprising:

detecting a signal at a first node, the signal having a first voltage magnitude;

comparing the first voltage magnitude to a reference voltage magnitude;

if the first voltage magnitude is less than the reference voltage magnitude,

transferring the signal with the first voltage magnitude to a second node; and

if the first voltage magnitude is greater than the reference voltage magnitude,

reducing the first voltage magnitude to a second voltage magnitude less than or equal to the reference voltage magnitude; and

transferring the signal with the second voltage magnitude to the second node.

23. The method of claim 22 further comprising:

providing a supply voltage for the integrated circuit; and

providing a magnitude of the supply voltage for the reference voltage magnitude.

24. The method of claim 23 further comprising:

providing the magnitude of the supply voltage equal to approximately zero.

25. The method of claim 23 further comprising:

providing the magnitude of the supply voltage greater than zero.

26. The method of claim 23 further comprising:

varying the magnitude of the supply voltage from zero to greater than zero.

27. The method of claim 22 wherein:

reducing the first voltage magnitude further comprises:

conducting a current across a resistor to reduce the first voltage magnitude to the second voltage magnitude.

28. The method of claim 27 wherein:

reducing the first voltage magnitude further comprises:

turning on a transistor to conduct the current across the resistor.

29. The method of claim 22 further comprising:

operating the integrated circuit in a suspend mode;

detecting a different signal at the first node, the different signal having a third voltage magnitude;

comparing the first voltage magnitude to a different reference voltage magnitude;

if the third voltage magnitude is less than the different reference voltage magnitude,

transferring the different signal with the third voltage magnitude to the second node; and

if the third voltage magnitude is greater than the different reference voltage magnitude,

reducing the first voltage magnitude to a fourth voltage magnitude less than or equal to the different reference voltage magnitude; and

transferring the different signal with the fourth voltage magnitude to the second node.

30. The method of claim 22 further comprising:

operating the integrated circuit in a suspend mode;

detecting a different signal at the first node, the different signal having a third voltage magnitude;

comparing the first voltage magnitude to a different reference voltage magnitude;

if the third voltage magnitude is less than the different reference voltage magnitude,

transferring the different signal with the third voltage magnitude to the second node; and

if the third voltage magnitude is greater than the different reference voltage magnitude,

reducing the first voltage magnitude to a fourth voltage magnitude less than or equal to the reference voltage magnitude; and

transferring the different signal with the fourth voltage magnitude to the second node.